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DESCRIPTION

SEMICONDUCTOR INTEGRATED DEVICE HAVING SOLID-STATE IMAGE
SENSOR PACKAGED WITHIN AND PRODUCTION METHOD FOR SAME

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TECHNICAL FIELD

The present invention relates to a semiconductor
integrated device having a solid-state image sensor packaged
10 within and a production method for the same.

BACKGROUND ART

Recently, chip size packages have been widely used in
15 order to miniaturize the chip size of solid-state image
sensors.

Firstly, a solid-state image sensor is described here.
FIG. 10 is a plan view showing the construction of a solid-
state image sensor.

20 A solid-state image sensor, in the case of a frame
transfer type for example, is essentially composed of a
light receiving section 200, a storage section 202, a
horizontal transfer section 204, an output section 206 and
an output amplifier 208. The light receiving section 200
25 has a plurality of light receiving pixels arranged in a
matrix, and stores information charges, which are generated
in response to receiving light, in each respective light
receiving pixel. The storage section 202 has a plurality of
storage pixels arranged according to the number of light
30 receiving pixels of the light receiving section 200, and
takes in and temporarily stores information charges of one
image stored in the light receiving section 200. The
horizontal transfer section 204 takes in information charges

from the storage section 202 in units of one line, and transfers them horizontally one pixel at a time. The output section 206 converts the information charges transferred from the horizontal transfer section 204 to voltage value and outputs them in units of one pixel. The output amplifier 208 amplifies the voltage value outputted from the output section 206, and outputs it as an image signal.

A solid-state image sensor having such a construction has a diffusion layer on the semiconductor substrate surface and electrodes arranged on the substrate, and comprises the light receiving section 200, the storage section 202, the horizontal transfer section 204, the output section 206 and the output amplifier 208, and lastly has a light-shielding film, which blocks light, arranged in all areas except for the light receiving section 200 (the hatched area in the diagram).

Next, a semiconductor integrated device in which a chip-sized package is applied for the solid-state image sensor is described. FIG. 11 is a cross-sectional view of the semiconductor integrated device cut along a position corresponding to the line X-X in FIG. 10.

A P-type diffusion layer 302 is formed on the surface of an N-type semiconductor substrate 300, and an N-type diffusion layer 304 is formed in this P-type diffusion layer 302. Highly concentrated P-type impurities are implanted in places in the N-type diffusion layer 304, and a channel stopper (not shown) is formed. Then, a transfer electrode 306 is formed on the semiconductor substrate 300 having an insulation film 305 in between, and the solid-state image sensor is formed.

An insulation film 308 is laminated on the transfer electrode 306, and a voltage supply line 310 and a pad electrode 322 are formed on this insulation film 308. This

voltage supply line 310 and pad electrode 322 are electrically connected to the transfer electrode 306 via a contact formed in the insulation film 308. Moreover, an insulation film 312 is laminated on the voltage supply line 310 and the pad electrode, and an internal wiring 314 is formed on the insulation film 312. This internal wiring 314 is, on its cross-sectional surface, connected to an external wiring 110 arranged along the side face of the package. An insulation film 316 is laminated on the internal wiring 314, and a light-shielding film 318 is arranged in the area covering the storage section 202, the horizontal transfer section 204 and the output section 206 on this insulation film 316. Then, a surface protection film 320, covering the light-shielding film 318 and the insulation film 316, is formed.

DISCLOSURE OF THE INVENTION

The contact resistance of the connection place, between the internal wiring 314 of the sensor and the external wiring 110, needs to be kept sufficiently low. Usually, the thickness of the voltage supply line is approximately 1 μ m, and as this thickness is insufficient to directly connect to the external wiring 110, an additional internal wiring 314 having greater thickness has needed to be provided.

In this case, since an additional process for forming the internal wiring 314 is required, production throughput of the solid-state image sensor is reduced, and the problem of a rise in production cost had arisen.

Also, the end part of the internal wiring 314 can easily become corroded from outside the sensor and there has been the problem of a reduction in the strength of the connection with the external wiring 110 when corroded.

In consideration of the problems of the conventional art mentioned above, an object of the present invention is to provide a semiconductor integrated device that is capable of solving at least one of abovementioned issues, and that does not undermine the characteristics of the sensor, and that can be formed easily; and a production method for the same.

The present invention is a semiconductor integrated device comprising: a solid-state image sensor having on a semiconductor substrate, a light receiving section which receives light and generates information charges, and a transfer section which transfers information charges stored in the light receiving section; and wherein a voltage is supplied through a pad electrode arranged along one edge of the semiconductor substrate; a light-shielding film which is formed on the semiconductor substrate and which shields at least some part of the transfer section from light; a first wiring formed in the same layer as the light-shielding film, with one end connected to the pad electrode and an other end extended to a side edge of the semiconductor substrate; a second wiring arranged to go around a side face of the semiconductor substrate, and connected to the first wiring; and a sealing member which seals the solid-state image sensor.

Another aspect of the present invention is characterized in that in a production method for a semiconductor integrated device in which an end part of a first wiring extends to a side edge of a solid-state image sensor, and in which this first wiring is connected to a second wiring arranged to go around a side face of the solid-state image sensor, the method includes: a first process in which a light receiving section which receives light and generates information charges, and a transfer

section which transfers information charges stored in the light receiving section, are formed, and then the solid-state image sensor is formed on the semiconductor substrate; a second process in which a light-shielding film which shields at least the transfer section, is formed on the semiconductor substrate, and the first wiring is formed in the same layer as the light-shielding film; and a third process in which the second wiring is formed and connected to the first wiring.

Another aspect of the present invention is characterized in that in a production method for a semiconductor integrated device in which an end part of an internal wiring extends to a side edge of a solid-state image sensor, and in which this internal wiring is connected to an external wiring arranged to go around a side face of the solid-state image sensor, the method includes: a first process in which a light receiving section which receives light and generates information charges, and a transfer section which transfers information charges stored in the light receiving section, are formed, and then the solid-state image sensor is formed on the semiconductor substrate; a second process in which a pad electrode which supplies voltage to the light receiving section and to the transfer section, is formed while a first internal wiring is formed in the same layer as the pad electrode; a third process in which a light-shielding film which shields at least the transfer section, is formed on the semiconductor substrate while the second internal wiring which overlaps the first internal wiring, is formed in the same layer as the light-shielding film; and a fourth process in which an external wiring is formed and then the first internal wiring and the second internal wiring are connected.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a view showing the cross-sectional construction of a semiconductor integrated device of an embodiment of the present invention.

5 FIG. 2A and FIG. 2B are perspective views showing the package appearance of the semiconductor integrated device of the embodiment of the present invention.

10 FIG. 3 is a flow chart illustrating a production method for the semiconductor integrated device of the embodiment of the present invention.

FIG. 4 is a diagram illustrating a production process of the semiconductor integrated device of the embodiment of the present invention.

15 FIG. 5 is a diagram illustrating the production process of the semiconductor integrated device of the embodiment of the present invention.

FIG. 6 is a diagram illustrating the production process of the semiconductor integrated device of the embodiment of the present invention.

20 FIG. 7 is a diagram illustrating the production process of the semiconductor integrated device of the embodiment of the present invention.

25 FIG. 8 is a diagram illustrating the production process of the semiconductor integrated device of the embodiment of the present invention.

FIG. 9 is a diagram illustrating the production process of the semiconductor integrated device of the embodiment of the present invention.

30 FIG. 10 is a plan view showing the construction of a conventional solid-state image sensor.

FIG. 11 is a view showing the cross-sectional construction of a conventional semiconductor integrated device.

BEST MODE FOR CARRYING OUT THE INVENTION

In connection with describing an embodiment of the present invention, firstly, the basic construction of a semiconductor integrated device having a solid-state image sensor packaged within is described.

FIG. 2A and FIG. 2B are perspective views showing one example of a semiconductor integrated device in which a chip-sized package is applied for the solid-state image sensor. A solid-state image sensor chip 104 is sealed between resin films 106, between a first and a second glass substrate 100 and 102. A plurality of ball-shaped terminals 108 are arranged on the main face of the second glass substrate, that is, the back side of the device, and these ball-shaped terminals 108 are connected to the solid-state image sensor chip 104 via an external wiring 110. A plurality of the external wirings 110 are connected to wirings drawn out from the solid-state image sensor chip 104, and establish contacts with each respective ball-shaped terminal 108.

Next, the embodiment of the invention of the present application is described. FIG. 1 is a view showing the cross-sectional construction of the semiconductor integrated device of the embodiment of the invention of the present application. FIG. 1 is a cross sectional view of a semiconductor integrated device cut at a position corresponding to the line X-X of FIG. 10. The same reference symbols are given to constructions the same as those shown in FIG. 2A, FIG. 2B, FIG. 10 and FIG. 11.

A P-type diffusion layer 302 is formed on an N-type semiconductor substrate 300, and an N-type diffusion layer 304 is formed in this P-type diffusion layer 302. Highly dense P-type impurities are partially implanted in the N-

type diffusion layer 304 and a channel stopper (not shown) is formed. Then, a transfer electrode 306 is arranged on the semiconductor substrate 300 having the insulation film 305 in between.

5 An insulation film 308 is laminated on the transfer electrode 306, and a voltage supply line 310 and a first internal wiring 407 are formed on this insulation film 308. This voltage supply line 310 and first internal wiring 407 are formed in the same layer, and of these, the first
10 internal wiring 407 is formed at the end part on the periphery side of the package.

 A second internal wiring 414 and a light-shielding film 418 are arranged on the voltage supply line 310, an pad electrode 322 and the first internal wiring 407, having an
15 insulation film 312 in between. The second internal wiring 414 is formed extending from a predetermined position to the end part of the package, and is made to connect to the first internal wiring 407 at the end part of the package. Moreover, the second internal wiring 414 is connected to an
20 external wiring 110 where it overlaps with the first internal wiring 407. A light-shielding film 418 is arranged to cover the area of the storage section 202, the horizontal transfer section 204 and the output section 206, and it prevents light from entering to the storage section 202, the
25 horizontal transfer section 204 and the output section 206. An insulation film 420 is laminated on the light-shielding film and the second internal wiring 414, and also, a first glass substrate 100 is arranged above them, sandwiching the resin film 106 in between.

30 According to this kind of construction, the contact area of the external wiring 110 and the internal wiring becomes greater compared to that of the conventional construction, so that the connection strength between the

external wiring 110 and the internal wiring can be improved. Also, since the second internal wiring 414 that constitutes part of the internal wiring is formed in the same layer as the light-shielding film 418, the second internal wiring 414 can be formed at the same time while using the forming process of the light-shielding film 418. Consequently, the connection strength between the external wiring 110 and the internal wiring can be improved without incurring additional production process.

Furthermore, materials generally used for semiconductor devices, such as silver, gold, copper, aluminum, nickel, titanium, tantalum, and tungsten, may be used as the chief material for the voltage supply line 310, the pad electrode 322 and the light-shielding film 418. When taking into account electrical resistance value and processability of material, it is preferable to employ aluminum. Also, the end parts of the first internal wiring 407 and the second internal wiring 414 can easily become corroded from outside the sensor, and in order to avoid such corrosion, it is more preferable to employ aluminum containing copper in a range no less than 0.1 atomic percent and no more than 20 atomic percent.

Since the minimum process line width of the electrode needs to be kept small and the electrical resistance value needs to be kept sufficiently low, it is preferable that the thickness of the voltage supply line 310 and the pad electrode 322 be made no less than $0.5\mu\text{m}$ and no more than $2\mu\text{m}$. Moreover, it is even more preferable that it be made no less than $0.5\mu\text{m}$ and no more than $1\mu\text{m}$.

On the other hand, since the light-shielding film 418 does not require a minimum process line width made that small, and needs to sufficiently block unwanted light, it can be made thicker than the voltage supply wiring layer.

Taking into account the throughput of the production process, it is preferable that it be made no less than $1.5\mu\text{m}$ and no more than $8\mu\text{m}$ when aluminum is the chief material. Moreover, it is even more preferable that it be made no less than

5 $2.0\mu\text{m}$ and no more than $8\mu\text{m}$.

Specifically, the total thickness of the first internal wiring 407 and the second internal wiring 414, which is the connection point with the external wiring, is preferably made no less than $2\mu\text{m}$ at the least and no more than $10\mu\text{m}$,
10 and thus, the connection strength can be improved while the contact resistance when connected to the external wiring 110 on the side face of the solid-state image sensor is kept low, at the same level as that of the conventional internal wiring 314.

15 FIG. 3 is a flow chart describing a production method for the semiconductor integrated device of the invention of the present application, and FIG. 4 to FIG. 9 are cross-sectional views of the semiconductor integrated device, corresponding to each production process.

20 In step S10, the light receiving section 200 which is a sensor section, the storage section 202, the horizontal transfer section 204 and the output section 206 are formed. Firstly, P-type impurity ions are implanted and diffused in the surface of the N-type semiconductor substrate 300a in
25 wafer condition, and a P-type semiconductor area 302 is formed. Then, N-type impurity ions are implanted and diffused in the P-type semiconductor area 302 and an N-type semiconductor area 304 is formed. Then, the insulation film 305 and the transfer electrode 306 are formed on the
30 semiconductor substrate 300a by appropriately combining deposition techniques such as sputtering and a chemical vapor phase growth method, and photolithography techniques. Then, highly concentrated P-type impurity ions are implanted

in parts of the semiconductor area 304 to form the channel stopper (not shown), and the state as shown in FIG. 4 is reached.

5 In step S12, the peripheral circuit of the output amplifier 208 is formed in the area near the sensor section as shown in FIG. 5. Forming the peripheral circuit can be carried out in the same manner as the conventional process for forming a transistor.

10 For example, a source area and a drain area are formed by means of doping techniques such as thermal diffusion and ion implantation, and a thermally-oxidized film which becomes a gate insulation film is formed by means of thermal oxidation. Then, a polysilicon layer or a metal film, which becomes a source electrode (not shown), a drain electrode
15 (not shown) and a gate electrode, are formed by combining photolithography techniques and deposition techniques such as a chemical vapor phase growth method.

In step S14, the voltage supply line 310 and the first internal wiring 407 are formed as shown in FIG. 6. A metal
20 layer, which becomes the voltage supply line 310 that transmits externally supplied voltage, is formed. At the same time, the first internal wiring 407 is also formed making use of the metal layer.

Specifically, the interlayer insulation film 308 upon
25 which the voltage supply line 310 and the first internal wiring 407 are to be formed, is formed on the semiconductor substrate 300a. Then, aperture holes are provided in necessary places on the interlayer insulation film 308 by means of a photolithography technique, and the metal layer
30 is formed by means of a deposition technique such as sputtering or a chemical vapor phase growth method. Then, the voltage supply line 310 and the first internal wiring 407 are formed by patterning the metal layer.

For example, the metal layer can be formed by means of aluminum sputtering. In this case the voltage supply line 310 and the first internal wiring 407 can be formed to have high resistance to corrosion by employing aluminum

5 containing no less than 0.1 atomic percent and no more than 20 atomic percent of copper as the target material .

Furthermore, the voltage supply line 310 and the first internal wiring 407 can also be formed by using deposition. In this case, the voltage supply line 310 and the first
10 internal wiring 407 can be formed to have high resistance to corrosion by employing aluminum containing no less than 0.1 atomic percent and no more than 20 atomic percent of copper as the material at this point.

Furthermore, the voltage supply line 310 and the first
15 internal wiring 407 can be formed using a chemical vapor phase growth method. In this case, an aluminum film containing no less than 0.1 atomic percent and no more than 20 atomic percent of copper and having high corrosion resistance can be formed by adjusting the proportions of a
20 mix of an organic gas containing aluminum and an organic gas containing copper .

In step S16, the light-shielding film 418 and the second internal wiring 414 are formed as shown in FIG. 7.

Firstly, the interlayer insulation film 312 is formed.
25 Then, aperture holes are provided in necessary places on the sensor section and the peripheral circuit by means of a photolithography technique or similar, and the metal layer is formed by means of a vapor deposition technique such as sputtering or a chemical vapor phase growth method. Then,
30 the second internal wiring 414 and the light-shielding film 418 are formed by patterning the metal layer.

At this point, as with the voltage supply line 310, it is preferable to form the metal layer by means of sputtering,

vapor deposition or a chemical vapor phase growth method, and to form an aluminum film, containing no less than 0.1 atomic percent and no more than 20 atomic percent of copper, and having a high resistance to corrosion.

5 In step S20, the first and second glass substrates 100 and 102 are adhered by the resin films 106 as shown in FIG. 8. In the process of this step S20, for example, epoxy resin is generally used to adhere the glass plates.

10 In step S22, the external wiring 110 is formed as shown in FIG. 9. Firstly, an inverted V groove is formed by cutting from the second glass substrate 102 side using a tapered dicing saw, and the first and second internal wiring 407 and 414 are exposed out of the inner face of the groove. Then, a metal layer is formed on the inner face of the
15 groove by means of sputtering, vapor deposition, or a chemical vapor phase growth method, and the external wiring 110 is formed by patterning this metal layer. After this, the ball-shaped terminals 108 are formed so as to connect to the external wiring on the surface of the second glass
20 substrate 102.

 In step S24, the laminate formed in step S22 is diced along the scribe line; that is, the border line of each solid-state image sensor. As a result, the semiconductor integrated device is completed.

25 As described above, according to the production method for the semiconductor integrated device of the present embodiment, since the light-shielding film 418 and the internal wiring are formed in the same process, the process of forming the internal wiring can be omitted compared to in
30 the conventional production method. Consequently, the production process can be simplified, and the solid-state image sensor package can be efficiently produced. Also, since internal wiring is formed in two stages for the first

and second internal wirings 407 and 414, and has a two-layer construction, the connection strength with the external wiring 110 can be improved.

According to the present invention, in a semiconductor
5 integrated device in which the internal wiring is connected to the external wiring arranged along the side face of the package, a semiconductor integrated device, for which the production process can be simplified without undermining the characteristics of the sensor, and a production method for
10 the same can be provided.

Furthermore, although a frame transfer type solid state image sensor was indicated as the example for this embodiment, it is not limited to this. For example there is ample possibility for application with semiconductor
15 integrated devices using interline type or frame-interline type solid state image sensors too.